Amendments to the Specification

Please replace Paragraph **[0004]** in the application as published with the following rewritten paragraph:

[0004] Performance and economic factors of integrated circuit design and manufacture have caused the scale of elements (e.g. transistors, capacitors and the like) of integrated circuits to be drastically reduced in size and increased in proximity on a chip. That is, increased integration density and proximity of elements reduces the signal propagation path length and reduces signal propagation time and susceptibility to noise and increase of possible clock rates while the reduction in element size necessary for increased integration density increases ~~to~~ the ratio of functionality which can be provided on a chip (approaching, if not achieving, a "system on a chip") to the costs of production (e.g. wafer/chip area and process materials) per chip and, potentially, the cost of devices containing the chips by reducing the number of inter-chip and inter-board connections required in a complete apparatus.

Please replace Paragraph **[0006]** in the application as published with the following rewritten paragraph:

[0006] At extremely small size regimes currently and foreseeably of interest (e.g. about 60 nm channel length and smaller), performance of FETs is often degraded by so-called short channel effects unless special structures such as extension and/or halo implants are employed to maintain acceptable levels of performance. However, the difference in physical behavior of dopants for semiconductors used to produce different conductivity types of transistors presents substantial difficulties in manufacture of FETs, particularly including such structures having acceptable electrical performance at acceptable manufacturing yields. In particular, boron is generally used for extension and source/drain implants in pFETs and in halo implants in nFETs (sometimes with indium) while arsenic (and/or phosphorus) is used for the extension and source/drain implant structures in nFETs and halo implants in pFETs. While arsenic diffuses sufficiently slowly in silicon at annealing temperatures to allow shallow and abrupt ~~junction s~~ junctions to be maintained at the source, and

drain of nFETs, boron diffuses at a much faster rate at the same temperatures. The faster diffusion rate of boron causes the tip of the impurity region of extension implants to spread under the transistor gate, shortening the channel further and increasing the junction depth within the silicon, compromising a shallow channel geometry that allows the channel conductivity to be suitably controlled at low gate threshold voltages. Therefore, there is a trade-off between low resistance extensions and source/drain regions which require a high temperature activation annealing process and shallow junctions to maintain suitable switching thresholds and avoid undesirable rolloff effects (e.g. a reduction of switching threshold with reduction of channel length) which can lead to unacceptably low switching thresholds at short channel lengths.

Please replace Paragraph **[0011]** in the application as published with the following rewritten paragraph:

[0011] Additionally, junction capacitance (Cj) is a major parasitic element which arises from the depletion charge between the source/drain implant and the oppositely doped substrate ~~and~~ which contributes to switching delay in CMOS circuits and is a significant part of the output capacitance in bulk CMOS circuits. Limitation of junction capacitance has been approached through use of expensive silicon-on-insulator structures which have an inherently lower junction capacitance than bulk FETs. In bulk FETs, implants have been used to reduce junction capacitance by developing graded junctions. However, at particularly small feature size regimes, boron diffusivity in the horizontal direction increases process parameter criticality in nFETs where boron is used (sometimes with indium) for the halo implants. In pFETs, lateral diffusion of the source/drain implants can reduce the perimeter component of junction capacitance by compensating the halo implant, thereby eliminating the p-n junction between the source/drain and the halo which reduces the overall junction capacitance. However, excessive boron diffusion in the vertical direction can lead to an increase in the area component of junction capacitance. Thus, if the lateral diffusion of boron in the source/drain region can be increased without causing increased overlap capacitance and, simultaneously, the vertical diffusion of boron in the source/drain region can be minimized, then junction

capacitance can be significantly reduced. The increase in junction capacitance with increased compressive forces from shallow trench isolation (STI) structures has been reported and attributed to change in band gap in "Stress-Induced Increase in Reverse Bias Junction Capacitance" by V. P. Gopinath et al., IEEE Electron Device Letters, Vol. 23, No. 6, June 2002. This effect is not considered to be fully understood but could possibly be explained by either stress-induced alteration of vertical diffusion of impurities or stress induced band gap change with compressive force as the author of the article proposes or a combination thereof. In any case, the use of STI or other structures providing a compressive force across transistors for the purpose of reducing boron diffusivity compromises transistor performance by increasing junction capacitance.

Please replace Paragraph **[0028]** in the application as published with the following rewritten paragraph:

[0028] The effects of stressed film 100 on the rate of boron diffusion (as simulated) are depicted in FIG. 3B, approximately corresponding to the region identified by dashed line 35 of FIG. 2. The simulations depict boron concentrations after annealing at approximately 1000°C. for a duration sufficient to activate the implanted impurities. For comparison, the simulation of FIG. 3A assumes an unstressed film 100' otherwise identical to stressed film 100 of FIG. 3B. It can readily be seen that diffusion 50 under the gate 14 is much reduced in comparison with diffusion 40 of FIG. 3A and largely maintained ~~with~~ within the region of compression extending under the gate as depicted in FIG. 2. Further, while the boron concentration generally spreads and results in an angled gradient of impurity concentration under film 100' and a relatively large vertical diffusion distance 60 in FIG. 3A, the boron diffusion under stressed film 100 has a much more nearly vertical gradient and uniform thickness of the implanted and diffused region with a much smaller vertical diffusion distance (e.g. 70). The reduction in diffusivity thus achieved for boron sufficient to prevent compromise of pFET electrical characteristics by excessive boron diffusion.

Please replace Paragraph **[0030]** in the application as published with the following rewritten paragraph:

[0030] It should also be appreciated that such an effect can be achieved by only two additional process steps beyond those usually required for production of a transistor having a structure similar to that of FIG. 1. That is, after the basic steps of forming isolation structures (e.g. STI), forming a gate oxide layer, forming patterned gate electrodes, reox (forming a thin oxide to round lower corners of the gate oxide), separate nFET and pFET extension and halo implants, spacer formation and separate nFET and pFET S/D implants but before the impurity activation anneal, tensile layer 100 is formed. Then the anneal process is carried out while the pFET S/D regions are under compressive stress from the tensile film 100 (which stress is substantially increased during annealing, as alluded to above). Then, after annealing is complete, tensile film 100 is removed and the transistor completed in a known manner but which may include application of other stressed films or other stressed structures to enhance carrier mobility as disclosed in U.S. patent applications Ser. Nos. 10/695,752, 10/695,754, or 10/695,748, (IBM docket numbers FIS920030190, FIS920030191 and FIS920030264US1) filed Oct. 30, 2003, which are hereby fully incorporated by reference. Thus, the meritorious effects of the invention can be achieved by the inclusion of the steps of adding and removing a stressed film wherein adequate stresses can be achieved at temperatures of about 600°C. that does not cause significant diffusion, even of boron, during formation of the stressed film 100.

Please replace Paragraph **[0034]** in the application as published with the following rewritten paragraph:

[0034] Referring now to FIG. 8, a film stack 200 preferably comprising a layer of unstressed oxide 210 followed by a layer 220 of tensile nitride or oxynitride is applied. The first layer 210 should be as thin as possible and a thickness of about 50Å is preferred and sufficient for the practice of the invention. This layer is primarily provided to facilitate later removal of the overlying stressed layer and, for that reason, should be of a material which resists etching by etchants suitable for removal of the stressed layer and also etchable selectively to the underlying material. It also appears, from the experimental results which will be discussed below, that layer 210, when used in combination with a highly stressed tensile film 220 may alter the distribution of stresses somewhat from that of FIG. 2 to yield a somewhat different distribution of

boron that may be advantageous in some circumstances. The thickness of the tensile layer 220 should be determined as discussed above.

Please replace Paragraph **[0036]** in the application as published with the following rewritten paragraph:

[0036] A unique aspect of this invention is that by applying a stressed film at this point in the process, a structure comprising the stressed film directly on top of the thin SiO_2 layer and/or Si with a high dose of boron in the range of 2×10^{15} to 6×10^{15} atoms/cm^2 is formed. Directly adjacent to the high dose ~~boron~~ region of boron is a less highly doped region of boron of about 1.5×10^{14} to about 3 to 5×10^{14} atoms/cm^2 located directly under the source/drain spacers. The peak region of the halo implant, typically arsenic, is located underneath the lightly doped extension region. The geometry prior to annealing is shown in FIG. 7.